Amendments to the Claims

1. (Original) In an integrated circuit system having access to a reference data table for holding information used to control at least one circuit block in said system and at least one of a power supply circuit, a body bias control circuit, a clock delivery circuit, a temperature monitor circuit, and a configuration control circuit, a method of improving the performance of said system comprising

(A) obtaining system performance data by testing said system at different supply voltages, different body-bias voltages, different clock speeds, different temperatures, different data bus widths, different circuit block configurations, or combinations thereof; and

(B) entering values based on said data into said reference data table, where at least one of said power supply circuit, said body bias control circuit, said clock delivery circuit, said temperature monitor circuit, and said configuration control circuit is controlled using said values.

2. (Original) A method according to Claim 1 wherein said system is tested at different supply voltages.

3. (Original) A method according to Claim 1 wherein said system is tested at different body-bias voltages.

4. (Original) A method according to Claim 1 wherein said system is tested at different clock speeds.

5. (Original) A method according to Claim 1 wherein said system is tested at different temperatures.

6. (Original) A method according to Claim 1 wherein said reference data

contains data for the entire system.

7. (Original) A method according to Claim 1 wherein said reference data table contains data for one or more circuit blocks.

8. (Original) A method according to Claim 1 wherein said reference data table is not on the same chip as the circuits controlled using data in said reference data table.

9. (Original) A method according to Claim 1 wherein said system is one chip.

10. (Original) A method according to Claim 9 wherein said system is tested when it is on a wafer.

11. (Original) A method according to Claim 1 wherein said power supply circuit is adjusted using said values.

12. (Original) A method according to Claim 1 wherein said clock delivery circuit is adjusted to minimize skew using said values.

13. (Original) A method according to Claim 12 wherein said clock delivery circuit has a delay locked loop circuit.

14. (Original) A method according to Claim 1 wherein said temperature monitor circuit data is adjusted using said values.

15. (Original) A method according to Claim 1 wherein said system contains at least two blocks that can perform the same function and the block assigned to perform that function is determined using said values.

16. (Original) A method according to Claim 1 wherein at least one but not all of said power supply circuit, said body bias control circuit, said clock delivery circuit, said temperature monitor circuit, and said configuration control circuit is

controlled using designed values.

17. (Original) A method according to Claim 1 wherein said test includes 2 to 4 different supply voltages between 1 and 4 volts at 2 to 4 different body-bias voltages between -0.5 and +0.5 volts and 2 to 4 different clock speeds between 1 and 300 MHz at a maximum and a minimum desired temperature.

18. (Original) A method according to Claim 1 wherein said test includes 2 to 4 different supply voltages between 1 and 4 volts at 2 to 4 different body-bias voltages between -0.5 and +0.5 volts and 2 to 4 different clock speeds between 0.2 and 2 GHz at a maximum and a minimum desired temperature.

19. (Original) A method according to Claim 1 wherein said data is used to adjust a MEMS component in said system.

20. (Original) A method according to Claim 1 wherein said reference data table is programmable.

21. (Original) A method according to Claim 1 wherein said values are permanently entered into said reference data table.

22. (Original) A chip made according to the method of Claim 1.

23. (Original) A computer comprising at least one chip according to Claim 22.

24. (Original) In an integrated circuit system having a programmable reference data table for holding information used to control at least one of operation voltage, operating clock speed, and temperature range in a power supply circuit, a body bias control circuit, a clock delivery circuit, a temperature monitor circuit, and a configuration control circuit, a method of improving the performance of said system comprising

(A) obtaining system performance data by testing said system at different supply voltages, different body-bias voltages, different clock speeds, different temperatures, different data bus widths, different circuit block configurations, or combinations thereof; and

(B) entering values based on said data into said reference data table, where at least one of said operation voltage, operating body-bias voltage, operating clock speed, and temperature range in said power supply circuit, body bias control circuit, clock circuit, clock delivery circuit, temperature monitor circuit, and configuration control circuit is controlled using said values.

25. (Original) A chip made according to the method of Claim 24.

26. (Original) A computer comprising at least one chip according to Claim 25.

27. (Original) In an integrated circuit system having access to a reference data table, at least two same function circuit blocks, and a control circuit to control which of said circuit blocks executes a task, based on values in said reference data table, a method of improving the performance of said system comprising

(A) obtaining system performance data by testing said system at different supply voltages, different body-bias voltages, different clock speeds, different temperatures, different data bus widths, different circuit block configurations, or combinations thereof; and

(B) entering values based on said data into said reference data table, whereby said control circuit selects or configures one of said blocks based on values in said reference data table.

28. (Original) A method according to Claim 27 wherein at least one of said circuit blocks is on a different chip.

29. (Original) A chip made according to the method of Claim 27.

30. (Original) A computer comprising at least one chip according to Claim 29.

31. (New) A method according to Claim 1 wherein data is entered into said reference data table by a non-volatile memory method.

32. (New) A method according to Claim 19 wherein data is entered into said reference data table post-silicon.

33. (New) A MEMS device having a programmable reference table in which data is entered after fabrication of said MEMS.

34. (New) A MEMS device according to Claim 33 that has temperature monitor circuit.

35. (New) A MEMS device according to Claim 33 wherein said MEMS and said programmable reference table are on different chips.

36. (New) A MEMS device according to Claim 33 wherein said programmable reference table contains applied voltage data for said MEMS.

37. (New) In an integrated circuit system having access to a reference data table for holding information used to control at least one circuit block in said system and at least one of a power supply circuit, a body bias control circuit, a clock delivery circuit, a temperature monitor circuit, and a configuration control circuit, the improvement comprising a reference data table having values based on system performance data obtained by testing said system at different supply voltages, different body-bias voltages, different clock

speeds, different temperatures, different data bus widths, different circuit block configurations, or combinations thereof entered into said reference data table, where at least one of said power supply circuit, said body bias control circuit, said clock delivery circuit, said temperature monitor circuit, and said configuration control circuit is controlled using said values.

38. An integrated circuit system according to Claim 37 wherein data is entered into said reference table post-silicon.

39. An integrated circuit system according to Claim 37 wherein data is entered into said reference table by a non-volatile memory method.

40. An integrated circuit system according to Claim 37 wherein said integrated circuit system comprises one chip.